APPENDIX C

(CLEAN VERSION OF ALL PENDING CLAIMS)

(Serial No. 09/912,982)

CLAIMS

What is claimed is:

1. An apparatus for selectively applying different amounts of pressure to a plurality of locations on a backside of a substantially circular semiconductor device structure, comprising:

a support structure configured to receive the semiconductor device structure;

a plurality of pressurization rings within said support structure, each of said plurality of pressurization rings being configured to apply pressure to a correspondingly annular region of the backside of the semiconductor device structure assembled with said support structure; and

a plurality of magnetic controllers, each of said plurality of magnetic controllers associated with a corresponding one of said plurality of pressurization rings.

2. The apparatus of claim 1, wherein each of said plurality of pressurization rings comprises a magnetized material.

3. The apparatus of claim 2, wherein each of said plurality of magnetic controllers is positioned adjacent said corresponding one of said plurality of pressurization rings and is oriented to repel said corresponding one of said plurality of pressurization rings.

4. (Amended) The apparatus of claim 2, wherein each of said plurality of magnetic controllers is positioned opposite the semiconductor device structure assembled with said support structure from said corresponding one of said plurality of pressurization rings and is oriented to attract said corresponding one of said plurality of pressurization rings.

5. The apparatus of claim 1, wherein each of said plurality of pressurization rings comprises a material that is attracted to a magnetic field.

6. The apparatus of claim 5, wherein each of said plurality of magnetic controllers is located so as to magnetically attract said corresponding one of said plurality of pressurization rings.

7. (Amended) The apparatus of claim 6, wherein, as at least one pressurization ring of said plurality of pressurization rings is attracted toward a corresponding one of said plurality of magnetic controllers, said at least one pressurization ring is configured to be biased against and to apply pressure to the backside of the semiconductor device structure at a corresponding annular region thereof.

8. The apparatus of claim 5, wherein said material comprises a ferrous material.

9. The apparatus of claim 5, wherein said material comprises a magnetized material.

10. The apparatus of claim 1, wherein each of said plurality of magnetic controllers comprises an electromagnet.

11. The apparatus of claim 1, wherein each of said plurality of magnetic controllers is configured to be moved toward and away from said corresponding one of said plurality of pressurization rings.

12. The apparatus of claim 1, wherein each of said plurality of magnetic controllers is configured to bias said corresponding one of said plurality of pressurization rings against corresponding annular regions of the backside of the semiconductor device structure with a variable magnitude of force.

13. (Amended) An apparatus for selectively applying different amounts of pressure to a plurality of locations on a backside of a semiconductor device structure, comprising:

a support structure configured to receive the semiconductor device structure;

a plurality of independently movable pressurization structures located within said support structure, each of said pressurization structures located and oriented adjacent a region on a backside of a semiconductor device structure assembled with said support structure; and

a plurality of actuators, each of said plurality of actuators associated with a corresponding pressurization structure of said plurality of pressurization structures so as to bias said corresponding pressurization structure against the backside of the semiconductor device structure assembled with said support structure.

14. (Amended) The apparatus of claim 13, wherein each of said plurality of pressurization structures comprises a ring.

15. The apparatus of claim 13, wherein each of said plurality of actuators comprises a magnetic controller.

16. (Amended) The apparatus of claim 15, wherein each of said plurality of pressurization structures comprises a magnetized material.

17. (Amended) The apparatus of claim 15, wherein each of said plurality of pressurization structures comprises a material that is attracted to a magnetic field.

18. The apparatus of claim 15, wherein each of said plurality of actuators is oriented so as to repel a corresponding pressurization structure.

19. The apparatus of claim 15, wherein each of said plurality of actuators is oriented so as to attract a corresponding pressurization structure.

20. The apparatus of claim 15, wherein each of said plurality of actuators comprises an electromagnet.

21. The apparatus of claim 15, wherein each of said plurality of actuators is movable toward and away from a corresponding pressurization structure.

22. The apparatus of claim 15, wherein each of said plurality of actuators comprises a vacuum source.

23. (Amended) The apparatus of claim 22, further comprising a spring associated with each of said plurality of independently movable pressurization structures, each said spring biasing a corresponding pressurization structure against the backside of the semiconductor device structure, each of said plurality of actuators being configured to pull a corresponding one of said plurality of independently movable pressurization structures away from the backside of the semiconductor device structure.

24. The apparatus of claim 15, wherein each of said plurality of actuators comprises a positive pressure source.

25. (Amended) The apparatus of claim 24, further comprising a spring associated with each of said plurality of independently movable pressurization structures.

26. (Amended) The apparatus of claim 24, wherein said positive pressure source is configured to bias a corresponding pressurization structure against the backside of the semiconductor device structure assembled with said support structure.

27. (Amended) The apparatus of claim 15, wherein each of said plurality of actuators is configured to bias said corresponding pressurization structure against the backside of the semiconductor device structure assembled with said support structure with variable amounts of force.

28. (Amended) The apparatus of claim 18, wherein each of said plurality of actuators is located to force said corresponding pressurization structure against the backside of the semiconductor device structure assembled with said support structure.

29. (Amended) The apparatus of claim 19, wherein each of said plurality of actuators is located to pull said corresponding pressurization structure against the backside of the semiconductor device structure assembled with said support structure.

30. (Amended) The apparatus of claim 15, wherein each of said of pressurization structures has associated therewith a spring.

31. A method for polishing or planarizing a surface of a semiconductor device structure, comprising:

selectively applying a plurality of different amounts of pressure to different, selected locations of a backside of the semiconductor device structure; and

polishing or planarizing at least one layer on the surface of the semiconductor device structure.

32. The method of claim 31, wherein said selectively applying said plurality of different amounts of pressure comprises biasing independently movable pressurization structures against the backside of the semiconductor device structure.

33. The method of claim 32, wherein said biasing comprises magnetically biasing said independently movable pressurization structures against said backside.

34. The method of claim 33, wherein said magnetically biasing comprises magnetically repelling said independently movable pressurization structures toward said backside.

35. The method of claim 33, wherein said magnetically biasing comprises magnetically attracting said independently movable pressurization structures toward said backside.

36. The method of claim 32, wherein said biasing comprises resiliently biasing said independently movable pressurization structures against said backside.

37. (Amended) The method of claim 36, wherein said selectively applying comprises selectively applying a negative pressure to at least one of said independently movable pressurization structures.

38. The method of claim 32, wherein said biasing comprises applying a positive pressure to at least one of said independently movable pressurization structures.

39. The method of claim 31, wherein said polishing or planarizing comprises chemical-mechanical polishing.

40. The method of claim 31, wherein said selectively applying a plurality of different amounts of pressure and said polishing or planarizing together effect the formation of a substantially planar surface on the semiconductor device structure.

41. (Amended) The method of claim 31, further comprising locating at least one raised area on an active surface of the semiconductor device structure.

42. (Amended) The method of claim 41, wherein said selectively applying a plurality of different amounts of pressure comprises applying an appropriate amount of pressure to said backside of the semiconductor device structure, opposite said at least one raised area thereof so as to planarize said active surface during said polishing or planarizing.

43. The method of claim 41, wherein said selectively applying a plurality of different amounts of pressure comprises selectively applying pressure to a backside of another semiconductor device structure of the same type as said semiconductor device structure, opposite a location of said at least one raised area of said semiconductor device structure.

44. The method of claim 43, wherein said polishing or planarizing comprises forming a substantially planar surface on the semiconductor device structure.

45. (Amended) The method of claim 31, wherein said plurality of different amounts of pressure is substantially simultaneously applied to said backside of said semiconductor device structure.

46. (Amended) A method for polishing at least one layer on a semiconductor device structure, comprising:

polishing at least one layer of a first semiconductor device structure;

locating any raised areas on said first semiconductor device structure following said polishing;

selectively applying pressure to a backside of at least one second semiconductor device structure of a same type as said first semiconductor device structure, said selectively applying being effected at locations beneath areas of said at least one second semiconductor device structure that correspond to said raised areas of said first semiconductor device structure; and

at least mechanically polishing at least one layer of said at least one second semiconductor device structure.

47. (Amended) The method of claim 46, wherein said locating comprises employing metrology techniques.

48. The method of claim 46, wherein said selectively applying comprises applying a sufficient amount of pressure at each of said locations to form a substantially planar surface on said at least one second semiconductor device structure.

49. The method of claim 46, wherein said selectively applying comprises selectively applying different amounts of pressure at different ones of said locations.

50. The method of claim 46, wherein said selectively applying comprises determining an appropriate amount of pressure to apply to each of said locations based on a height of each corresponding raised area.

51. The method of claim 46, wherein said selectively applying comprises selectively applying pressure to said backside of said at least one second semiconductor device structure at at least one annular location.

52. The method of claim 46, wherein said polishing comprises mechanically polishing said at least one layer of said first semiconductor device structure.

53. The method of claim 46, wherein said polishing comprises chemical-mechanical polishing said at least one layer of said first semiconductor device structure.

54. (Amended) The method of claim 46, wherein said at least mechanically polishing comprises chemical-mechanical polishing said at least one layer of said at least one second semiconductor device structure.

55. The method of claim 46, wherein said selectively applying comprises biasing at least one pressurization structure against said backside of said at least one second semiconductor device structure.

56. The method of claim 55, wherein said biasing comprises employing a magnet to bias said at least one pressurization structure against said backside.

57. The method of claim 56, wherein said employing said magnet comprises repelling said at least one pressurization structure toward said backside to effect said biasing.

58. The method of claim 56, wherein said employing said magnet comprises attracting said at least one pressurization structure toward said backside to effect said biasing.

59. The method of claim 55, wherein said biasing comprises resiliently biasing at least one pressurization structure against said backside.

60. (Amended) The method of claim 59, wherein said selectively applying further comprises applying a negative pressure to said at least one pressurization structure.

61. The method of claim 55, wherein said biasing comprises applying a selected amount of positive pressure to said at least one pressurization structure.

62. A system for polishing a semiconductor device structure, comprising:

a metrology component for detecting any raised areas on an active surface of the semiconductor device structure;

a support structure configured to secure the semiconductor device structure;

a pressurization component including:

a plurality of independently movable pressurization structures; and

actuators corresponding to each of said plurality of pressurization structures, said actuators each being configured to bias a corresponding pressurization structure against a backside of the semiconductor device structure with a selected amount of force; and

a polishing component.

63. The system of claim 62, wherein each of said plurality of pressurization structures comprises a magnetized material.

64. The system of claim 62, wherein each of said plurality of pressurization structures comprises a material that is attracted to a magnetic field.

65. The system of claim 64, wherein each of said plurality of pressurization structures comprises a ferrous material.

66. The system of claim 64, wherein each of said plurality of pressurization structures comprises a magnetized material.

67. The system of claim 62, wherein each of said plurality of pressurization structures has an annular shape.

68. (Amended) The system of claim 62, wherein each of said actuators comprises a magnetic controller.

69. The system of claim 68, wherein each said magnetic controller comprises a magnet.

70. The system of claim 69, wherein each said magnetic controller comprises an electromagnet.

71. The system of claim 69, wherein each said magnetic controller is oriented and located so as to repel a corresponding pressurization structure toward a backside of a semiconductor device structure assembled with said support structure.

72. The system of claim 69, wherein each said magnetic controller is oriented and located so as to attract a corresponding pressurization structure toward a backside of a semiconductor device structure assembled with said support structure.

73. The system of claim 62, wherein said actuators comprise a positive pressure source.

74. The system of claim 62, wherein said actuators comprise a negative pressure source.

75. (Amended) The system of claim 74, wherein said pressurization component further comprises at least one spring associated with each of said plurality of independently movable pressurization structures.

76. (Amended) The system of claim 75, wherein said at least one spring biases a corresponding pressurization structure against said backside.

77. The system of claim 76, wherein said negative pressure source is configured to withdraw said corresponding pressurization structure away from said backside.

78. The system of claim 62, wherein each actuator is configured to bias a corresponding pressurization structure against a backside of a semiconductor device structure assembled with said support structure with variable amounts of force.

79. The system of claim 62, wherein said polishing component comprises a mechanical polishing apparatus.

80. The system of claim 62, wherein said polishing component comprises a chemical-mechanical polishing apparatus.

81. The system of claim 62, wherein said polishing component includes assembled therewith a rotatable polishing pad.

82. (Amended) The system of claim 62, wherein said polishing component includes an element for rotating the semiconductor device structure in a plane thereof and relative to a polishing pad assembled with said polishing component.

83. (Amended) A method for polishing or planarizing a surface of a semiconductor device structure, comprising:

polishing a first semiconductor device structure;

analyzing a topography of an active surface of said first semiconductor device structure;

generating a force gradient based on said analyzing;

applying said force gradient to a backside of at least one second semiconductor device structure; and

polishing said at least one second semiconductor device structure with said force gradient applied to said backside thereof.

84. The method of claim 83, wherein said polishing said first semiconductor device structure comprises CMP.

85. The method of claim 83, wherein said analyzing comprises employing a metrology technique.

86. The method of claim 83, wherein said generating comprises:

considering a height of at least one raised area on said active surface of said first semiconductor device structure; and

considering a rate of material removal from a lowermost area of said active surface of said first semiconductor device structure.

87. The method of claim 86, wherein said generating further comprises determining amounts of force to apply to at least two areas of said backside of said at least one second semiconductor device structure so as to facilitate the formation of a substantially planar active surface of said at least one second semiconductor device structure during said polishing thereof.

88. (Amended) The method of claim 83, wherein said applying said force gradient comprises applying at least two different amounts of pressure to said backside.

89. The method of claim 83, wherein said polishing said at least one second semiconductor device structure comprises chemical-mechanical polishing.

90. (Amended) A method for compensating for nonplanarities on an active surface of a semiconductor device structure during polishing thereof, comprising:

polishing at least one layer of a first semiconductor device structure;

analyzing a topography of an active surface of said first semiconductor device structure;

selectively applying increased amounts of pressure to at least two locations on a backside of at least one second semiconductor device relative to pressure applied to other areas of said backside, said at least two locations corresponding to raised areas on said active surface of said first semiconductor device structure following said polishing of at least one layer thereof; and

polishing said at least one second semiconductor device structure as said selectively applying is being effected.

91. (Amended) The method of claim 90, wherein said selectively applying comprises applying a pressure gradient to said backside of said at least one second semiconductor device structure.

92. (Amended) The method of claim 91, comprising generating said pressure gradient based at least partially on:

a height of at least one raised area on said active surface of said first semiconductor device structure following said polishing of said at least one layer of said first semiconductor device structure; and

a rate of material removal from a lowermost area on said active surface of said first semiconductor device structure following said polishing of said at least one layer of said first semiconductor device structure,

said height and said rate together indicating another rate and pressure for removing material from said at least one raised area to provide a substantially planar active surface on said first semiconductor device structure.

93. (Amended) The method of claim 90, wherein said polishing said at least one layer of said first semiconductor device structure comprises chemical-mechanical polishing.

94. The method of claim 90, wherein said polishing said at least one second semiconductor device structure comprises chemical-mechanical polishing.